```
? show files
File  15:ABI/Inform(R) 1971-2006/Feb 03
         (c) 2006 ProQuest Info&Learning
File  16:Gale Group PROMT(R) 1990-2006/Feb 03
         (c) 2006 The Gale Group
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         (c)2006 The Gale Group
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 275:Gale Group Computer DB(TM) 1983-2006/Feb 03
         (c) 2006 The Gale Group
File 621:Gale Group New Prod.Annou.(R) 1985-2006/Feb 03
         (c) 2006 The Gale Group
File   9:Business & Industry(R) Jul/1994-2006/Feb 02
         (c) 2006  The Gale Group
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         (c) 2006 Business Wire.
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         (c) 2006 PR Newswire Association Inc
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         (c) 2006 McGraw-Hill Co. Inc
File 634:San Jose Mercury  Jun 1985-2006/Feb 02
         (c) 2006 San Jose Mercury News
File 636:Gale Group Newsletter DB(TM) 1987-2006/Feb 03
         (c) 2006 The Gale Group
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         (c) 1999 Business Wire
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         (c) 1999 PR Newswire Association Inc
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         (c) 2006 Institution of Electrical Engineers
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         (c) 2006 ProQuest Info&Learning
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         (c) 2006 BLDSC all rts. reserv.
File  99:Wilson Appl. Sci & Tech Abs 1983-2005/Dec
         (c) 2006 The HW Wilson Co.
File 256:TECINFOSOURCE 82-2005/DEC
         (c) 2006 INFO.SOURCES INC
File 474:New York Times Abs 1969-2006/Feb 02
         (c) 2006 The New York Times
File 475:Wall Street Journal Abs 1973-2006/Feb 02
         (c) 2006 The New York Times
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 The Gale Group
? ds

Set     Items   Description
S1     993813   PROBE OR PROBES OR WAFER OR WAFERS
S2   24059177   DESIGN??? OR CUSTOM????????
S3      62431   S1 (10N) S2
S4    1019910   VERIF???????
S5       4179   S3 AND S4
S6    2035218   SIMULAT???? OR REPLICAT????
S7    4351554   VERIF??????? OR VALID????? OR INSPECT????
S8      12003   S3 AND S7
```

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S9         5580   S6 (10N) S1
S10      223802   S6 (10N) S2
S11         199   S8 AND S9 AND S10
S12         123   S11 NOT PY>2002
S13     8088297   TEST???
S14      312361   WAFER OR WAFERS
S15       21120   S13 (6N) S14
S16          15   S12 AND S15
S17           9   RD  (unique items)
?
```

? t s17/medium,k/1-9

17/K/1 (Item 1 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

10195391 Supplier Number: 87781670 (USE FORMAT 7 FOR FULLTEXT)
Q- and V-band MMIC low noise amplifiers. (Technical Feature).(Statistical Data Included)
Jang, Byung-Jun; Yom, In-Bok; Lee, Seong-Pal
Microwave Journal, v45, n6, p74(6)
June, 2002
Language: English Record Type: Fulltext
Article Type: Statistical Data Included
Document Type: Magazine/Journal; Refereed; Trade
Word Count: 2735

... the active device models, the need of EM simulation, etc. First of all, accurate and **verified** active device models are needed. MMIC LNA designs at V-band often require smaller devices...

...is prone to give a misleading model, caused by the selection of a non-representative **wafer** that can degrade **design** robustness, (5)
In order to circumvent the scaling and extrapolation problems, and to predict small...

...width should be done using scaling equations provided with the model. Scaling equations are normally **valid** for gate widths from 75 to 125 percent of the original gate width. (9)
The...

...noise figure. The distributed device model described in the previous section was linked to the **simulator** and employed in the **design** . Amplifiers were **designed** at Q- and V-bands.
A photograph of the V-band amplifier is shown in...only for DC biasing to minimize the sensitivity to process variations. For ease of on-**wafer testing** , the amplifiers were **designed** to operate with one common drain and one common gate bias.
An important focus in the **design** is the electromagnetic (EM) **simulation** because the layout is very densely integrated to reduce the MMIC size. Therefore, all the...

...the V-band amplifier was 2.2 by 1.5 mm.
After completing the EM **simulation** and final layout, the yield performance of the **designed** amplifier was calculated. To explain yield reasonably, a long-term database of one-fingered elementary devices from 90 **wafers** was used. Inserting these values into the LIBRA **simulator** 's discrete-value data file, a realistic yield variation can be calculated.
The Q-band...
...thick GaAs substrates. The small-signal S-parameters and noise parameters of the amplifiers were **tested** with on- **wafer** probing. The measured and **simulated** performances of the V-band amplifier are presented in Figure 5. They compare very favorably...396-398.
(4.) M.D. Dufault and A.K. Sharma, "Millimeter-wave HEMT Noise Models **Verified** through V-band," IEEE MTT-Symposium Digest, 1996, pp. 1321-1324.
(5.) M. King, et...

17/K/2 (Item 2 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

09955021 Supplier Number: 89805190 (USE FORMAT 7 FOR FULLTEXT)
Manufacturing, test to designers: We need to talk -- Semicon West speakers call for dialogue on key issues. (integrated circuit product and test equipment)
Wilson, Ron
Electronic Engineering Times, p1
July 29, 2002
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1485

... it is not uncommon to have a design meeting that includes not only the chip **design** team but the lithography team, the stepper people and the **wafer** -processing team as well. They will work together to cut down the risks and reduce...

...using the most expensive mask-writing equipment with the lowest throughput, performing the most exhaustive **inspections** and attempting repairs on every identifiable defect. And it means $1 million mask sets.
Often...
...are critical. So everything gets the full treatment.
A similar example comes up in mask **inspection** . At 130 nm and below, many defects that are detectable on the mask would be...

...to decide whether to attempt to repair the defect, the mask shop would have to **simulate** the impact of the defect on the **wafer** (tools for doing so are now available from Numerical Technologies), extract circuit parameters from the **simulation** and then ask the **design** team if the new circuit was acceptable. Such information loops are rare today.
Neither does...much narrower lines in order to prevent its being polished away."
The issues continue through **wafer** processing and into **test** , where **test** engineers are already pleading for access to design information, particularly about the designer's original intent.
The problem in test is similar to the problem in mask **inspection** : When you detect a failure, how do you know whether it is a fatal problem...

...specific defect-caused failure modes in a chip, and analog test, which attempts not to **inspect** a circuit but to characterize it. Increasingly, faults in finished dice are delay faults or...

...for-test or automatic test pattern generation data that increasingly forms the information flow between **design** and test.
A two-way street
In mask making, lithography, **wafer** processing and **test** , experts are calling for increased dialogue with the design team. They emphasize that the information...

17/K/3 (Item 3 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

08517136 Supplier Number: 73041206 (USE FORMAT 7 FOR FULLTEXT)
Analysis of a 200/300mm vertical furnace with integrated metrology.
Claasen-Vujcic, Tanja; Hasper, Albert; Abraham, Michael
Solid State Technology, v44, n4, pS6
April, 2001
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Refereed; Trade
Word Count: 3051

... metrology units for measurements on patterned wafers. This will result in a significant reduction of **test wafer** consumption and will thus have a major impact on cost of ownership. Currently, **test wafers** in 300mm fabs can contribute more than 30% to the overall cost of ownership of...

...value of 0.05nm. This positive result was expected due to the compact, low mass **design** . For the same reason, sensitivity to vibrations is negligible.

Simulation objectives and tools

The real performance of a system can be analyzed well only in... needed has been determined with the help of logistic simulations. It is assumed that particle **inspection** is done on one product **wafer** and thickness measurement on three **test wafers** /batch of 100 **wafers** . It is also important to determine the scheduling rules used. We will analyze both modes...

...items have been analyzed: cycle time in the furnace area, scrap, yield, throughput, usage of **test wafers** , and capital investment.

Table 4 summarizes the results, and the rest of this article provides...

...total of 44 furnaces). This means about $4 million less capital investment for 300mm production.

Test wafer consumption. For the consumption of **test wafers** , it is in principle irrelevant whether the metrology takes place in a stand-alone unit or in an integrated unit. **Test wafer** costs can thus be assumed to be equal for both approaches. However, contribution of **test wafers** to the overall costs has become particularly significant in 300mm production. Therefore, reduction of **test wafer** consumption is a must for both approaches. A shift towards measurements on production wafers has ...

...a furnace (*)

Item	Requirement
System footprint	Not affected
System throughput	Not affected for common recipes
Test wafer consumption	(less than or equal to) stand-alone metrology

MTBF and MTBPM of metrology unit...

...next important milestone
is the development of a compact
ellipsometer for film measurements
on patterned **wafers** .
= Research/ **design**
= Qualification/ **testing**
= Production

Input for the **simulation** of the logic
fab and cost/ **wafer** calculation

	200mm	300mm
Cost/wafer		
Furnace cost	$800,000	$1,000,000
Metrology unit cost...		

17/K/4 (Item 4 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

08126118 Supplier Number: 67720102 (USE FORMAT 7 FOR FULLTEXT)
Broadening the platforms for system-in-package solutions.
Truzzi, Claudio; Lerner, Steve
Solid State Technology, v43, n11, p115
Nov, 2000
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Refereed; Trade
Word Count: 2766

... apply solder balls to the bottom side, 6) singulate the packages, 7) laser mark and **inspect** , and 8) perform final functional test.
Figure 8 shows an RF functional block realized with...

...wire bonding and encapsulation are still there, but new capabilities needed include system-level interconnect **design** and characterization, system **simulation** , final **test** , and even **wafer** processing tools for **wafer** -level packaging and thin-film substrate fabrication.
CLAUDIO TRUZZI received his degree in electrical engineering...

17/K/5 (Item 5 from file: 16)
DIALOG(R)File 16:Gale Group PROMT(R)

04350554 Supplier Number: 46380860 (USE FORMAT 7 FOR FULLTEXT)
Static-timing analysis speeds verification
Electronic Engineering Times, p76
May 13, 1996
Language: English Record Type: Fulltext
Document Type: Magazine/Journal; Trade
Word Count: 1355

(USE FORMAT 7 FOR FULLTEXT)
Static-timing analysis speeds verification
TEXT:
...complex that ASIC designers are spending 50 to 75 percent of the design cycle on **verification** . As a result, there is a trend toward splitting the **verification** effort, so that functionality is **verified** with simulation and timing is **verified** with static-timing analysis (STA). In recognition of this trend, LSI Logic has integrated STA...
Traditionally, system **designers** have **verified** timing with dynamic analysis during **simulation** . One capability provided by DTA is margin analysis, which takes into account such parameters as...

...hold times.
DTA also provides dither and scale analyses, which are very important

for design **verification** . Dither analysis assures the system engineer that a design is not sensitive to a tester's pin-to-pin skew, while scale analysis slows the **design** so that it can be **tested** at the **wafer** level.

Another important use for DTA is **simulating** best and worst-case timing "corner cases" while varying the ASIC process, system voltage and operation temperature.

Dynamic-timing **simulation** for comprehensive timing analysis has traditionally been used for **designs** with lower complexity levels. This technology supports both synchronous and asynchronous designs. It also can ...

...heavily dependent upon the completeness of the vector set. For complex system-on-a-chip **designs** , it is virtually impossible to develop and **simulate** comprehensive timing test vectors.

Further, clock and data in corner cases do not track each...
...these structures, external data signal transitions directly cause state transitions. Such structures are difficult to **verify** with closed-form methods because they have implied constraints on intersignal stability.

For STA, designers...

...STA tools support their analysis.

Bidirectional buses pose special challenges to both STA and functional **verification** because they can create logic loops and false paths. Techniques such as case analysis, which...

...the source. Designers are not prohibited from using ZCPs, and STA tools can detect and **validate** their timing; however, they must be functionally **verified** .

Down a false path

One well-known limitation with STA is the false-path problem...

...paths that are false.

Therefore, the existence of all designer-declared false paths must be **verified** . This is commonly done using simulation tools because most available STA tools have problems identifying...

...from false ones. However, LSI Logic has found that Quad Design's Motive (Modular Timing **Verifier**) employs techniques that can efficiently understand and minimize the analysis of false paths.

Because the...

...are also included.

The increasing complexity of system-on-a-chip designs calls for the **verification** features of both static- and dynamic-timing analysis. Computer system applications are largely synchronous and thus are ideal for STA alone, while communications **designs** include asynchronous structures that require dynamic-timing **simulation** as a complement to the STA.

STA and DTA are driven from descriptions originally defined...

...using VHDL or Verilog-based descriptions. At the RTL level, fundamental functionality and timing are **verified** through dynamic **simulation** . Analyzing at the RTL level makes fundamental **design** flaws visible to system engineers early in the design cycle, thus improving designer efficiency and...a minimal amount of functional simulation. This balance of predominantly static-timing analysis and functional **verification** can be effective for design **verification** , testability analysis and manufacturing test.

As a result, most extensive simulation can be removed from...
...logic, such as state machines, pipelines and asynchronous logic interfaces.

This combined timing simulation and **verification** process includes enough steps to guarantee that the device will satisfy all **design** specifications and also that the test program meets requirements. **Simulation** regression test vectors are generated at the RTL level and used at the gate level...

17/K/6 (Item 1 from file: 148)

08677073 SUPPLIER NUMBER: 18295325 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Static-timing analysis speeds verification . **(Technology Information)**
Zarrinfar, Farzad; Potter, Vern
Electronic Engineering Times, n901, p76(2)
May 13, 1996
ISSN: 0192-1541 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 1502 LINE COUNT: 00128

Static-timing analysis speeds verification . **(Technology Information)**

...ABSTRACT: complexity of system-on-a-chip designs has resulted in ASIC designers splitting the lengthy **verification** cycle so that functionality is **verified** with simulation and timing is **verified** with static-timing analysis (STA). LSI Logic has responded to this trend by integrating STA...

...and timing violations. For many designs, STA's balance of static-timing analysis and functional **verification** is sufficient for design **verification** , manufacturing test and testability analysis.

TEXT:

...complex that ASIC designers are spending 50 to 75 percent of the design cycle on **verification** . As a result, there is a trend toward splitting the **verification** effort, so that functionality is **verified** with simulation and timing is **verified** with static-timing analysis (STA). In recognition of this trend, LSI Logic has integrated STA...

Traditionally, system **designers** have **verified** timing with dynamic analysis during **simulation** . One capability provided by DTA is margin analysis, which takes into account such parameters as...

...hold times.

DTA also provides dither and scale analyses, which are very important for design **verification** . Dither analysis assures the system engineer that a design is not sensitive to a tester's pin-to-pin skew, while scale analysis slows the **design** so that it can be **tested** at the **wafer** level.

Another important use for DTA is **simulating** best and worst-case timing "corner cases" while varying the ASIC process, system voltage and operation temperature.

Dynamic-timing **simulation** for comprehensive timing analysis has traditionally been used for **designs** with lower complexity levels. This technology supports both synchronous and asynchronous designs. It also can ...

...heavily dependent upon the completeness of the vector set. For complex

system-on-a-chip **designs** , it is virtually impossible to develop and **simulate** comprehensive timing test vectors.

Further, clock and data in corner cases do not track each...

...these structures, external data signal transitions directly cause state transitions. Such structures are difficult to **verify** with closed-form methods because they have implied constraints on intersignal stability.

For STA, designers...

...STA tools support their analysis.

Bidirectional buses pose special challenges to both STA and functional **verification** because they can create logic loops and false paths. Techniques such as case analysis, which...

...the source. Designers are not prohibited from using ZCPs, and STA tools can detect and **validate** their timing; however, they must be functionally **verified** .

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Therefore, the existence of all designer-declared false paths must be **verified** . This is commonly done using simulation tools because most available STA tools have problems identifying...

...from false ones. However, LSI Logic has found that Quad Design's Motive (Modular Timing **Verifier**) employs techniques that can efficiently understand and minimize the analysis of false paths.

Because the...

...are also included.

The increasing complexity of system-on-a-chip designs calls for the **verification** features of both static- and dynamic-timing analysis. Computer system applications are largely synchronous and thus are ideal for STA alone, while communications **designs** include asynchronous structures that require dynamic-timing **simulation** as a complement to the STA.

STA and DTA are driven from descriptions originally defined...

...using VHDL or Verilog-based descriptions. At the RTL level, fundamental functionality and timing are **verified** through dynamic **simulation** . Analyzing at the RTL level makes fundamental **design** flaws visible to system engineers early in the design cycle, thus improving designer efficiency and...a minimal amount of functional simulation. This balance of predominantly static-timing analysis and functional **verification** can be effective for design **verification** , testability analysis and manufacturing test.

As a result, most extensive simulation can be removed from...

...logic, such as state machines, pipelines and asynchronous logic interfaces.

This combined timing simulation and **verification** process includes enough steps to guarantee that the device will satisfy all **design** specifications and also that the test program meets requirements. **Simulation** regression test vectors are generated at the RTL level and used at the gate level...

17/K/7 (Item 1 from file: 275)

01466951 SUPPLIER NUMBER: 11260825 (USE FORMAT 7 OR 9 FOR FULL TEXT)
CrossCheck testability solution extended with interface to ATE. (CrossCheck Technology Inc.'s CX-Probe) (product announcement)
Tuck, Barbara
Computer Design, v30, n12, p46(2)
Sept, 1991
DOCUMENT TYPE: product announcement ISSN: 0010-4566 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT; ABSTRACT
WORD COUNT: 1259 LINE COUNT: 00102

TEXT:
...days or hours, according to CrossCheck. Until now, the CrossCheck solution has consisted of a **test** -point matrix on the base **wafer** that functions as an on-chip grid of sense **probes** , and the CX-Test fault **simulation** and automatic test program generation (ATPG) software (see "High-density ASICs force focus on testability...
... its CrossCheck-based LFT150K gate arrays (see "CrossCheck testability reaches commercial gate array family," Computer **Design** , March 1, p 48).
The workstation-based CX- **Probe** software uses the outcome of ATE to diagnose functional failures in ASIC devices incorporating the...

...V.sub.ss] and [V.sub.dd] faults; CAD errors such as mask faults; and **design** errors in macrocell libraries.
CX- **Probe** , which has no inherent limitation on the size of the device it analyzes, requires a Sun 4, Sparcstation 1 or Sparcstation 2. Memory use depends on the number of **simulation** and test vectors, which vary with **design** complexity. The software operates with almost any modern ATE, according to CrossCheck, via a suitable...

...netlists and functional patterns in either Verilog or LSI Logic's Lsim format.
Few early **customers** expected
It's expected that **customers** for CX- **Probe** will initially be limited to CrossCheck's ASIC partners who will use the diagnostic software ...

...analysis of life-test, burn-in, and field failures. The long-term benefit of CX- **Probe** , though, lies in its being a tool that **customers** will be able to buy to look at system problems themselves, according to Bill Alexander...

...shipped prototypes, it's questionable whether a field failure is an LSI Logic or a **customer** 's problem," says Alexander. If **customers** have CX-**Probe** , Alexander suggests, they can debug field failures themselves and thus manage their complex designs at...

...LSI Logic nor Fujitsu have actually used CX-Probe yet, its promise hasn't been **validated** as of presstime. Benchmark data will soon be available from Raytheon which has been beta...

17/K/8 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

05117227 INSPEC Abstract Number: B9205-2570-014, C9205-7410D-030

Title: Validating **an ASIC standard cell library**
Author(s): Agatstein, W.; McFaul, K.; Themins, P.
Author Affiliation: Intel Corp., Chandler, AZ, USA
Conference Title: Proceedings. Third Annual IEEE ASIC Seminar and Exhibit (Cat. No.90TH0303-8) p.P12/6.1-5
Editor(s): Hsu, K.W.; Schrader, M.E.
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA xviii+656 pp.
U.S. Copyright Clearance Center Code: TH0303-8/90/0000-P12-6.1$01.00
Conference Sponsor: IEEE
Conference Date: 17-21 Sept. 1990 Conference Location: Rochester, NY, USA
Language: English
Subfile: B C

Title: Validating **an ASIC standard cell library**
Abstract: The accurate **validation** of the CHMOS III and CHMOS IV cell-based libraries is discussed. The **validation** methodology consists of library test chips which isolate each cell in a measurable and meaningful circuit. These chips use the **customer** design, layout, and **simulation** environment, incorporating all library cells. Manufacturing the **test** chip **wafers** across the worst-case process corners further guarantees that **customer simulation** bounds silicon performance. The characterization process encompasses process, temperature, and voltage extremes. For customer-specific...
...Identifiers: **validation** methodology

17/K/9 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

03357427 INSPEC Abstract Number: B85001710
Title: A VLSI design methodology based on parametric macro cells
Author(s): Kriete, R.A.; Nettleton, R.K.
Author Affiliation: Harris Corp., Melbourne, FL, USA
Conference Title: ACM IEEE 21st Design Automation Conference Proceedings 84 (cat. no. 84CH2049-5) p.686-8
Publisher: IEEE, New York, NY, USA
Publication Date: 1984 Country of Publication: USA xx+717 pp.
ISBN: 0 8186 0542 1
U.S. Copyright Clearance Center Code: 0738-100X/84/0000-0686$01.00
Conference Sponsor: IEEE; ACM
Conference Date: 25-27 June 1984 Conference Location: Albuquerque, NM, USA
Language: English
Subfile: B

...Abstract: which can be modified by a computer program to meet the needs of a particular **design** . The **design** methodology, the chip layout, the **simulation** techniques, the **wafer testing** approach, and other software tools used to ensure a **valid** design are discussed.
...Identifiers: **wafer testing** ;
?